REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Claims 1, 3, 5, 31, and 32 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Fu in view of Sasaki. The rejection asserts that Fu shows a semiconductor device that is similar to the present application, except it does not have edges of the third opening being rounded off. Sasaki is cited to show the rounded edges on the third opening. Claims 1, 19, and new claims 38-40 now have been amended to define that the thickness of the first interlayer insulating film is less than one-third of the total thickness of the first and second insulating films. It is respectfully suggested that this feature may be patentable since the thickness of the first insulating film being greater than one-third of the total thickness allows a taper angle α to increase, and may result in difficulties in later etching steps. This is explained in the specification at page 10, lines 22-25. Both Fu and Sasaki fail to teach this feature that a thickness of the first interlayer insulating film is less than one-third of the total thicknesses of the first and second interlayer insulating films as claimed. Hence, even if Fu and Sasaki were combined, it is respectfully suggested that the claimed invention would not be obtained from this hypothetical combination.

Claims 2, 6-18, 33, and 34 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Fu in view of Sasaki and further in view of Lin. Claims 19-30 and 35-37 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Fu in view of Sasaki and Lin and further in view of Huang. These contentions are traversed for reasons set forth above. Lin is cited to show a taper angle β of the second interlayer insulating film with respect to a major surface of the semiconductor layer in the third opening being larger than that a taper angle α of the first interlayer insulating film with respect to the major surface of the layer in the second opening. Huang is cited to show an LDD region in a semiconductor. However, no cited reference discloses the semiconductor layer formed over the substrate having an insulating surface as defined in claims 6, 14, and 24. Even if the additional references are combined, it is respectfully suggested that this feature still is not taught or suggested.

In view of the above amendments and remarks, therefore, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 2/13/02

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VERSION TO SHOW CHANGES MADE

In the Claims:

New claims 38, 39, and 40 have been added.

Claims 1, 2, 10, 14, 19, and 24 have been amended as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor [layer] having at least channel, source and drain regions;

an insulating film formed on said semiconductor [layer];

a first interlayer insulating film over said insulating film;

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor [layer];

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said insulating film where surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor [layer], said portion of said insulating film and a portion of said first interlayer insulating film where surrounds said second opening,

wherein edges of at least said third opening are rounded off, and

wherein a thickness of the first interlayer insulating film is less than one third of total thickness of the first and second interlayer insulating films.

2. (Amended) A device according to claim 1 wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor [layer] in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to the major surface of said semiconductor [layer] in the second opening.

10. (Amended) A semiconductor device comprising:

a semiconductor [layer] having at least channel, source and drain regions;

an insulating film on said semiconductor [layer];

a first interlayer insulating film over said insulating film;

a second interlayer insulating film on said first interlayer insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor [layer];

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor [layer] and a

portion of said insulating film where surrounds said first opening;

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor [layer], said portion of said insulating film and a portion of said first interlayer insulating film where surrounds said second opening; and

an electrode formed on said first, second, and third openings and connected with one of said source and drain regions through said first, second, and third openings,

wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor [layer] in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to a major surface of said semiconductor [layer] in the second opening, and

wherein a thickness of the first interlayer insulating film is less than one third of total thickness of the first and second interlayer insulating films.

14. (Amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface and including at least channel, source and drain regions;

an insulating film on said semiconductor layer

multi-interlayer insulating films comprising at least an upper insulating layer and a lower insulating layer over said insulating film, said lower insulating layer comprising the same material as said upper insulating layer;

at least one contact hole in said multi-interlayer insulating films and said insulating film, said contact hole having a tapered section; and

an electrode formed on said contact hole and connected with one of said source and drain regions through said contact hole,

wherein a taper angle β of an inner surface of the upper insulating layer in the contact hole with respect to a major surface of said semiconductor layer is larger than a taper angle α of an inner surface of the lower insulating layer in the contact hole with respect to said major surface of said semiconductor layer.

19. (Amended) A semiconductor device comprising:

a semiconductor [layer] having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor [layer];

an interlayer insulating film comprising a plurality of insulating layers over said semiconductor layer and said insulating film; and

a contact hole in said interlayer insulating film and said insulating film for exposing a portion of said high doped impurity region, said contact hole has a tapered section,

wherein edges of said interlayer insulating film in said contact hole are rounded off, [and]

wherein angles of the tapered section of the contact hole decrease successively from a top interlayer insulating layer toward a bottom interlayer insulating layer, and

wherein a thickness of the bottom interlayer insulating film is less than one third of total thickness of the interlayer insulating film.

24. (Amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface and having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor layer;

an interlayer insulating film comprising a plurality of insulating layers over said semiconductor layer and said insulating film; and

a contact hole in said interlayer insulating film and said insulating film for exposing a portion of said high doped impurity region, said contact hole has a tapered section; and

an electrode formed on said contact hole and connected with one of said source and drain regions through said contact hole,

wherein edges of said interlayer insulating film in said contact hole are rounded off.